(3 Hours) **[Total Marks: 80]**

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

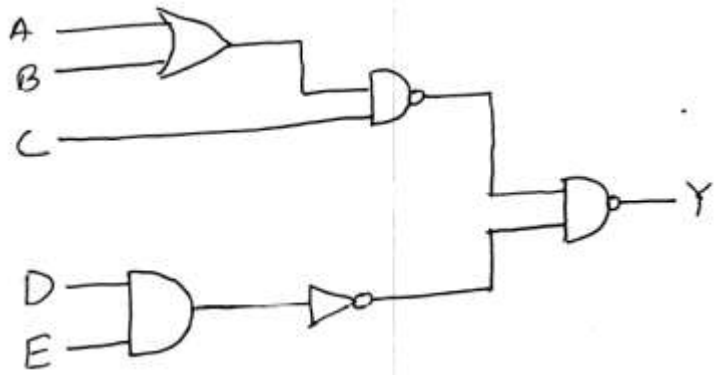
1. (a) Convert JK F/F to T F/F **(5)**
   (b) Explain current and voltage parameters of logic families. **(5)**
   (c) Design half adder circuit using gates. **(5)**
   (d) Prove the following Boolean theorem. $(A+\bar{A}B) = (A+B)$ **(5)**

2. (a) Explain Race around condition in JK F/F and explain how to avoid this condition. **(10)**
   (b) Convert $(27)_{10}$ & $(42)_{10}$ into binary, octal, hexadecimal, Excess-3 code and gray code. **(10)**

3. (a) Implement the following expression using 8:1 multiplexer. **(10)**
   $F(A, B, C, D)=\Sigma m (2,4,6,7,9,11,14)$
   (b) What is shift register? Explain any one type of shift register in detail. Give its applications. **(10)**

4. (a) Implement and explain 4 bit BCD adder using IC 7483 **(10)**
   (b) Design 3 bit synchronous counter using T F/F. **(10)**

5 (a) Find expression of Y for above logic diagram. **(10)**



   (b) Design 4 bit binary to Gray code converter **(10)**

6. (a) Explain following characteristics of logic families; **(10)**
   1. Propagation delay
   2. Noise margin
   3. Power Dissipation
   4. Fan out
   5. Figure of Merit
   (b) Draw K-map for following expression and implement using only Basic gates. **(10)**
   $F (A,B,C,D)= \Sigma m (0,3,6,9,10,12,14,15)$

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